

वैज्ञानिक तथा औद्योगिक अनुसंधान परिषद्
Council of Scientific & Industrial Research
राष्ट्रीय वांतरिक्ष प्रयोगशालाएं
National Aerospace Laboratories



CSIR - NAL Estd. 1959
ISO 9001 : 2015
Certified Organization

INVITATION FOR BIDS/NIT

Tender No. NAL/PUR/ALD/388/19-Y

Dated: 16-Dec-19

CSIR- National Aerospace Laboratories (NAL), Bengaluru, India is one of the premier laboratories under Council of Scientific and Industrial Research (CSIR), an autonomous body under Department of Scientific and Industrial Research, Government of India, New Delhi. CSIR-NAL is a Science and Knowledge based Research, Development and Consulting Organization. It is internationally known for its excellence in Scientific Research in Aerospace Engineering.

The Director, CSIR-NAL invites online quotation for procurement of the following item(s) for day to day research work.

Sl.No.	Description of Items	Unit	Quantity
01	Design and Development of Video Converter Card. Please refer Annexure for detailed specification.	Set	01

Single / Double Bid	Two Bid
Bid Security (EMD) (in INR)	Bid Security Declaration should be enclosed with quotation
Performance Security	10% of the purchase order value

01. Tender Documents may be downloaded from Central Public Procurement Portal <https://www.etenders.gov.in>. Aspiring Bidders who have not enrolled/ registered in e- procurement should enroll/ register before participating through the website <https://www.etenders.gov.in>. The portal enrolment is free of cost. Bidders are advised to go through instructions provided at 'Instructions for online Bid Submission'.
02. Tenderers can access tender documents on the website (For searching in the NIC site <https://www.etenders.gov.in>, kindly go to Tender Search option, select tender type and select ' Council of Scientific and Industrial Research' in organization tab and select NAL-Bengaluru-CSIR in department type Thereafter, Click on "Search" button to view all CSIR-NAL, Bengaluru tenders). Select the appropriate tender and fill them with all relevant information and submit the completed tender document online on the website <https://www.etenders.gov.in> as per the schedule given in the next page.
03. Either the Indian Agent on behalf of the Foreign principal or the Foreign principal can bid directly in a tender but not both. However, the offer of the Indian Agent should also accompany the authorization letter from their principal. To maintain sanctity of tendering system, one Indian Agent cannot represent two different Foreign principals in one tender.
04. Unsolicited / conditional / unsigned tenders (Quotations) shall not be considered. Quotations received after the due date and time shall be summarily rejected.
05. The Bidder shall comply the terms and conditions of the tender, failing which, the offer shall be liable for rejection.
06. The Director, CSIR- National Aerospace Laboratories., Bengaluru reserves the right to accept any or all the tenders either in part or in full or to split the order without assigning any reasons there for.


Raman Kumar
(Section Officer S&P)

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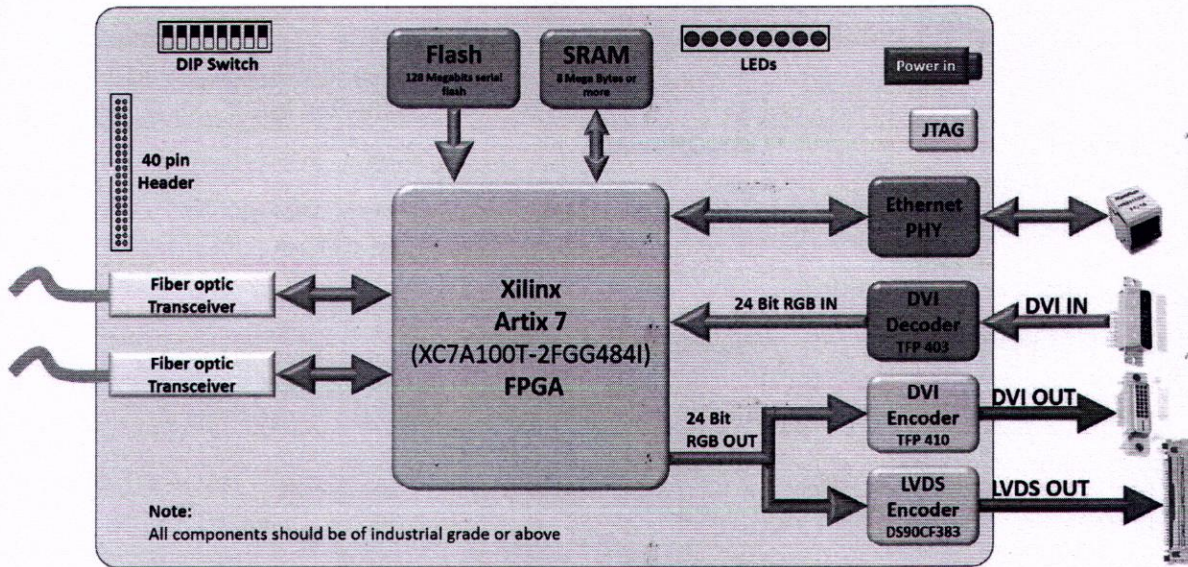
SCHEDULE CUM CRITICAL DATE SHEET

1	Name of Organization	CSIR-National Aerospace Laboratories, Bengaluru	
2	Tender Reference No	NAL/PUR/ALD/388/19-Y dated: 16-Dec-19	
3	Tender Type (Open/Limited/EOI/Auction/Single)	Open	
4	Type/Form of Contract (Work / Supply / Auction / Service / Buy / Empanelment / Sell)	Supply	
5	No of Covers (One/Two/Three/Four)	Two	
6	Tender Category (Services/Good/Works)	Goods	
7	Allow Resubmission (Only in online mode within scheduled period)	Yes	
8	Allow Withdrawal (Only in online mode within scheduled period)	Yes	
9	Allow Offline Submission	No	
10	Work Item Title	Design and Development of Video Converter Card.	
11	Work Description	Design and Development of Video Converter Card.	
12	Delivery Schedule	60 days from the date of purchase order	
13	Product Category (Civil Works / Electrical Works / Fleet Management / Computer Systems)	R & D Equipment	
14	Is Multi Currency Allowed	Yes	
15	a) Tender Publishing Date -	17-Dec-19	1800 Hrs
	b) Document Download Start Date-	17-Dec-19	1800 Hrs
	c) Bid Submission Start Date-	17-Dec-19	1800Hrs
	d) Bid Submission End Date-	09-Jan-20	1000 Hrs
	e) Bid Opening Date-	10-Jan-20	1100 Hrs
16	Bid Validity Days	90 days	
17	Address for communication	Stores and Purchase Officer CSIR-National Aerospace Laboratories, HAL Airport Road, Kodihalli, Bengaluru - 560017	
18	Inviting Officer	Director, CSIR-NAL	
19	Contact No	25086040, 25086041	
20	E-mail Address	purchaseek@nal.res.in	
21	Detailed specification of item	Refer Invitation for bids / NIT	
22	Tender Terms & Conditions & Instruction for online bid submission	The prospective bidders are requested to refer to the Standard Tender Document available on NAL Internet (www.nal.res.in) under the icon Tender-Purchase before formulating and submitting their bids	

Architecture and Specifications for the video converter card

Architecture

The architecture proposed for the video converter card is shown in the figure below;



Specifications

The proposed video converter card should meet the technical specifications detailed below.

1. Functional Specifications

- a. The converter card shall receive DVI-D input, decode and provide 24 bit RGB output to the FPGA for further processing.
- b. The converter card shall provide fibre-optic output.
- c. The converter card shall receive fibre-optic input, convert it to electrical signal and provide the same to the FPGA for further processing.
- d. The 24 bit RGB output provided by the FPGA shall be converted to DVI-D and routed out of the card through a DVI-D interface.
- e. The 24 bit RGB output provided by the FPGA shall be converted to LVDS and routed out of the card through a LVDS interface.
- f. The card shall provide a 10/100/1000 Ethernet interface for data communication/configuration/de-bugging.
- g. The DVI encoder and Decoder chip shall have hard wired configuration (*not through I2C*) for the defined specification above.
- h. The card shall provide a 40 header (*box type, polarised*) with power, ground and FPGA IOs connectivity.

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2. Operational Specifications

- a. The card shall have POWER ON indication.
- b. The card shall provide 8 LEDs with an interface to the FPGA for system status indication.
- c. The card shall have a ON-OFF switch for power control.

3. Electrical Specifications

Sl. No	Parameter	Specification	Remarks
1.	Power input	12v	240v to 12v adaptor, required for this card will have to be delivered by the vendor
2.	Power control	On-Off switch	
3.	Power indication	LED	

4. External Interface Specifications

Sl. No	Interface	Type	No. of channels
1.	Fiber-optic channels (SFPs)	In-Out	2
2.	Ethernet 10/100/1000	In-Out	1
3.	DVI-D	Input	1
4.	DVI-D	Output	1
5.	LVDS	Output	1
6.	FPGA IO (through a 40 pin header)	Power, Ground, Input, and Output	1
7.	JTAG port		1
8.	Power ON-OFF switch		1

5. Internal Interface Specifications**5.1. Fiber channel interface requirement:**

- a. Two standard SFP cage or small form factor fibre channel LC cable connectable connector.
- b. The differential lines for the Transmitter and the Receiver should be connected to FPGA.
- c. A throughput speed of greater than 6 Gbps should be achievable through Fibre optic connector and routing.

5.2. Ethernet interface requirement:

- a. The design should support 10/100/1000 Mbps Ethernet.
- b. The Ethernet PHY chosen should provide a GMII interface.
- c. The GMII interface of the PHY should be appropriately connected to the FPGA.

5.3. DVI-D receiver (input) interface requirement:

- a. TFP403 Texas instrument chip shall be used for DVI-D Receiver.
- b. FPGA to DVI-D receiver chip shall have a data rate of 165 MHz.
- c. The DVI-D receiver chip should be connected to FPGA with 24bit 1pixel/clock mode.

- d. The DVI-D receiver control signal such as HSync, VSync, Data enable and clock for the Video data should be connected to FPGA.
- e. I2C bus of the DVI Receiver should be disabled and the configuration should be done through hardware configuration of configuration pins.

5.4. DVI-D transmitter (output) interface requirement:

- a. TFP410 Texas instrument chip shall be used for DVI transmitter.
- b. FPGA to DVI Transmitter chip shall have a data rate of 165 MHz for 1pixel/clock or 400MHz for 2pixel/clock.
- c. The DVI Transmitter chip should be connected to FPGA with 24bit 1pixel/clock mode or 12bit 2pixel/clock mode.
- d. The DVI transmitter control signal such as HSync, VSync, Data enable and clock for the Video data should be connected to FPGA.
- e. I2C bus of the DVI Transmitter should be disabled and the configuration should be done through hardware configuration of configuration pins.

5.5. Memory interface requirement:

- a. Artix 7 FPGA compatible Flash of 128 Megabits or more should be interfaced to FPGA.
- b. Artix 7 FPGA compatible SRAM with a size of 8 Mega Bytes or more shall be interfaced to FPGA.

5.6. Power supply requirement

- a. External power supply shall be fed to board from an external 220v to 12v adapter (*to be provided by the vendor*).
- b. The necessary power rails for the components on the card shall be derived through DC-DC converters on the card.
- c. A power ON-OFF switch shall be provided on the card.

5.7. Other requirement:

- a. JTAG connector port shall be made available on the board.
- b. 8 LEDs connected to FPGA I/Os.
- c. 8-bit DIP switch, connected to FPGA.
- d. A 40pin 2.54 pitched DIL connector should be interfaced to FPGA
 - a. At least 2 clock capable pin.
 - b. 30 pins connected to FPGA I/Os
 - c. Four 3.3V power supply.
 - d. Four GND pins.

6. Connector Specifications

- a. The card shall provide standard SFP fibre optic transceiver connectors
- b. The card shall provide standard RJ-45 Ethernet connector
- c. The card shall provide standard 24+5 pins DVI-D female connectors for DVI-D input
- d. The card shall provide standard 24+5 pins DVI-D female connectors for DVI-D output
- e. The card shall provide standard LDVS connector
- f. 40 pin header for FPGA IO interface



7. Component Specifications

- a. The card shall use Xilinx Artix 7 (XC7A100T-2FGG484I) FPGA
- b. The card shall use 128 MB or higher flash memory with speed grade as appropriate for the FPGA used
- c. The card shall use Ethernet PHY with GMII interface to the FPGA
- d. The card shall use Texas Instruments TFP 403 DVI decoder
- e. The card shall use Texas Instruments TFP 410 DVI encoder
- f. The card shall use Texas Instruments DS90CF383 LVDS encoder

8. Protection Specifications

- a. The card shall have power transient protections
- b. The card shall have EMI/EMC protections
- c. Reverse polarity protection

9. Fabrication Specifications

- a. The NAL logo, card name and provision for Sl. No. shall be etched on the card in copper, on top layer.

10. Deliverables**1. Project Deliverables**

Sl. No.	Deliverable(s)	Remarks
1.	Fully functional video converter card hardware	03 Nos
2.	Associated cables; a. DVI-D cables b. LVDS cables	06 Nos. 03 Nos.
3.	Power supply adapter for the video converter card	03 Nos.
4.	VHDL test codes Note: 1. Only the codes which the vendor may use for testing the card and demonstrating the functionality of the interface to NAL needs to be delivered. 2. The specific VHDL code for the NAL's application of the card shall be developed by NAL.	1 set (in CD)
5.	Project files as detailed in subsequent sub-section	1 set (in CD)
6.	Documentation as detailed in subsequent sub-section	1 set (in print) 1 set (in CD)

2. Project files to be delivered in CD, as per item 5 of project deliverables Sl. No. 1 above.
 - a. Schematics – tool's native project folder with all files and settings
 - b. Schematic symbol library
 - c. Board design files - tool's native project folder with all files and settings

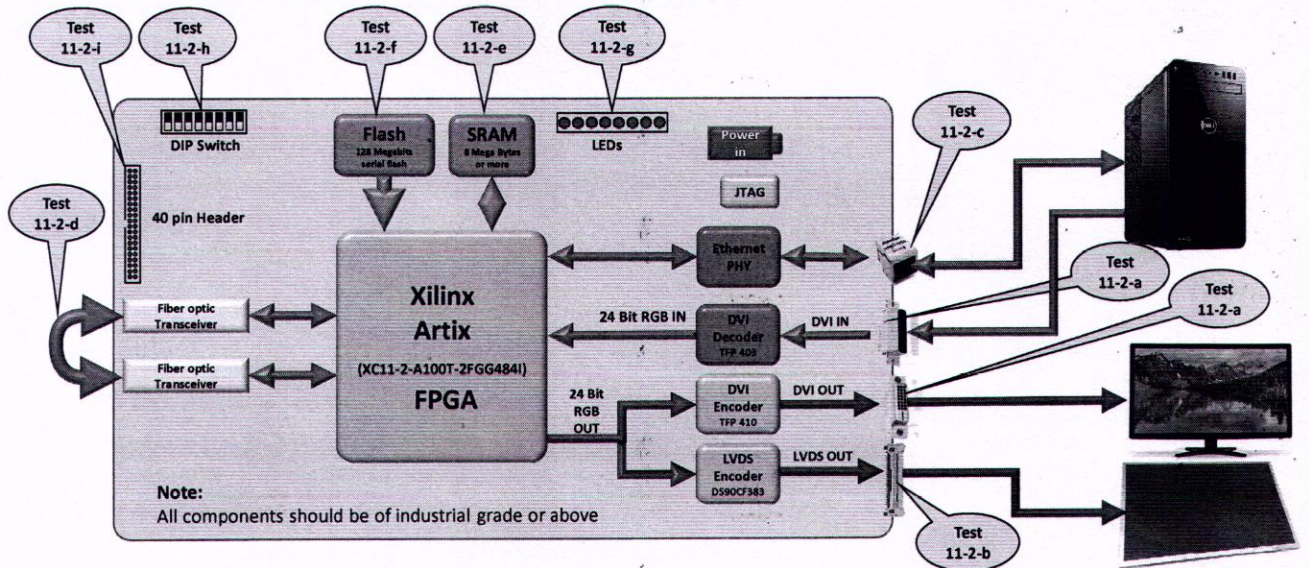
- d. Board design files – pdf in CD
- e. All component footprint library
- f. IBIS Models (*.ibs file used in SI Analysis)
- g. Gerber files
- h. PCB fabrication files
- i. PCB fabrication data including vendor details with alternate vendors list
- j. Bill of Materials (BOM) listing the OEM’s full part No., reseller’s part No. if applicable, alternate vendors (*min. 2 alternates*) with reseller details and costing
- k. VHDL files - tool’s native project folder with all files and settings

Note:

1. Only the codes which the vendor may use for testing the card and demonstrating the functionality of the interface to NAL needs to be delivered.
 2. The specific VHDL code for the NAL’s application of the card shall be developed by NAL.
3. Documentation to be delivered in CD, as per item 6 of project deliverables Sl. No. 1 above.
- a. Architecture Design (document in word & PDF and architecture diagram in PPT)
 - b. Components Data Sheet (including all capacitors and resistors with complete part number and footprint details in PDF)
 - c. Released Schematic Design (one copy of PDF)
 - d. Released Board Layout Design (one copy of PDF)
 - e. Released Gerber (one copy of PDF)
 - f. User manuals (hardware card and all test VHDL codes)

11. Acceptance Tests

1. The proposed test set is as depicted in the figure below.



2. Test to be demonstrated as part of acceptance procedure are as listed below.
- a. Receive video on DVI-D Input (*sent by a desktop PC*) and send it on DVI-D output to a DVI monitor. The tentative test setup is as shown in the figure above in Sl. No. 7, item 1.

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- b. Receive video on DVI-D Input (*sent by a desktop PC*) and send it on LVDS output to a LCD panel. The tentative test setup is as shown in the figure above in Sl. No. 7, item 1.
- c. Ethernet send/receive to PC/switch. The tentative test setup is as shown in the figure above in Sl. No. 7, item 1.
- d. Loopback test for testing Fibre channel interface.
- e. SRAM read/write test (*standard memory interface tests for address lines and data lines*).
- f. Boot from Flash test.
- g. LED tests
- h. DIP switch tests
- i. 40 pin GPIO In-Out tests

12. Delivery Schedule

The proposed video converter card is to delivered within 3 months from the date of PO.

✓



Tender No.: NAL/PUR/ALD/388/19-Y

BID-SECURING DECLARATION FORM

Date: _____

Bid No. _____

To (insert complete name and address of the purchaser)

I/We. The undersigned, declare that:

I/We understand that, according to your conditions, bids must be supported by a Bid Securing Declaration.

I/We accept that I/We may be disqualified from bidding for any contract with you for a period of one year from the date of notification if I am /We are in a breach of any obligation under the bid conditions, because I/We

(a)	have withdrawn/modified/amended, impairs or derogates from the tender, my/our Bid during the period of bid validity specified in the form of Bid; or
(b)	having been notified of the acceptance of our Bid by the purchaser during the period of bid validity (i) fail or reuse to execute the contract, if required, or (ii) fail or refuse to furnish the Performance Security, in accordance with the Instructions to Bidders.

I/We understand this Bid Securing Declaration shall cease to be valid if I am/we are not the successful Bidder, upon the earlier of (i) the receipt of your notification of the name of the successful Bidder; or (ii) thirty days after the expiration of the validity of my/our Bid.

Signed: (insert signature of person whose name and capacity are shown)
in the capacity of (insert legal capacity of person signing the Bid Securing Declaration).

Name: (insert complete name of person signing the Bid Securing Declaration)

Duly authorized to sign the bid for an on behalf of: (insert complete name of Bidder)

Dated on _____ day of _____ (insert date of signing)

Corporate Seal (where appropriate)

Note:

1. In case of a Joint Venture, the Bid Securing Declaration must be in the name of all partners to the Joint Venture that submits the bid.
2. Bid Security declaration must be signed in by the Proprietor/CEO/MD or equivalent level of Officer of the company.